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10/630,480	07/29/2003	Roberto Fabian Averbuj	030198	9692

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,480	AVERBUJ ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/05/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07/05/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered July 05, 2006.

- Claims 1-38 are pending. Claims 1, 26, & 28 are amended.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to amended claims 1, 26 & 28 and previously presented claims 2-25, 27 29-38 filed July 05, 2006 have been considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant's arguments and amendments with respect to the rejections under Ledford et al. US Pat no. 6,347,056 amended claims 1, 26 & 28 and previously presented claims 2-25, 27 29-38 filed July 05, 2006 have been considered but are moot in view of the new ground(s) of rejection.

The applicant contends that Crouch does not teach a centralized BIST controller for issuing commands for testing multiple memory modules. The examiner respectfully disagrees. Crouch states "In this case a single memory BIST controller creates the test stimulus and the test sequencing for all of the embedded memory arrays (the memory testing algorithms are embedded within the chip)" (column 1, lines 30-36). Further as seen clearly in Figure 1 clearly depicts a central BIST controller (130), testing a plurality of memory modules (140 & 150). As per the added limitation of a plurality of sequencers testing memory modules operating on different clock domains. Crouch

teaches "In this case, the memory test sequencer, stimulus generator, and comparator logic are all embedded within a single chip. Access to all of the individual memory arrays is provided" (column 2, lines 5-10). Hence, since more then one chip can be tested at one time, there will be a plurality of sequencers. Further "this test starts by loading sequential logic with a particular set of logic values (referred to as "DATA"), stopping the clock for a period of time, and then verifying the ability of the sequential logic to retain the first set of logic values. A second set of logic values, that are generally the complement of the first set ("DATABAR"), is then applied to the sequential logic, the clock is again stopped and re-started, and the sequential logic is verified again" (column 2, lines 25-30) and "if the memories are of different sizes (data width and address space), or in different frequency domains" (column 4, lines 35-50). Here clearly, it can be seen that the controller has the ability to control the clock, and since the memory modules 140 and 150 can be tested separately, they can be of different clock domains.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-24 & 26-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al. US Pat no. 5,995,731.

As per claim 1:

Crouch et al. teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 2 # 210 column 5, lines 55-60), that stores an algorithm for testing a plurality of memory modules (Figure 2 # 210), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (column 3, lines 55-59), and a plurality of sequencers that interpret the commands based on the command protocol (Figure 2 # 210 & 225, column 5, lines 51-55) and apply the generalized commands to the memory modules, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains (column 4, lines 35-50).

As per claim 2:

Crouch et al. teaches the system of claim 1 wherein the generalized commands specify the algorithm in accordance with the command protocol and without regard to timing requirements of the memory modules (column 6, lines 7-14).

As per claim 3:

Crouch et al. teaches the system of claim 1, wherein the generalized commands specify the algorithm without regard to physical characteristics of the memory modules (column 6, lines 7-14).

As per claim 4:

Crouch et al. teaches the system of claim 1, wherein each of the generalized commands includes a sequencer identifier that identifies one or more of the sequencers

to process the respective command and apply the command to the memory modules (column 6, lines 7-20).

As per claim 5:

Crouch et al. teaches the system of claim 4, wherein the sequencer identifier comprises a broadcast identifier to indicate that the generalized command is to be interpreted and applied by all of the distributed sequencers (column 7, lines 1-10).

As per claim 6:

Crouch et al. teaches the system of claim 4, wherein the sequencer identifier comprises a unicast identifier that identifies a specific one of the sequencers to interpret and apply the generalized command to the respective memory modules of the identified sequencer (column 7, lines 20-26).

As per claim 7:

Crouch et al. teaches the system of claim 4, wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes and a set of associated parameters (column 5, lines 51-60).

As per claim 8:

Crouch et al. teaches the system of claim 7, wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from address and data lines used during normal operation (column 6, lines 7-10).

As per claim 9:

Crouch et al. teaches the system of claim 7, wherein the set of defined operational codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters (column 5, lines 57-60).

As per claim 10:

Crouch et al. teaches the system of claim 9, wherein the parameters include a single-row (SR) field to direct the sequencers to apply the memory operations for all columns of the memory module of the respective memory modules for the sequencers that has a largest column-bit option while maintaining a row address at zero (column 4, lines 47-51).

As per claim 11:

Crouch et al. teaches the system of claim 9, wherein the parameters include an invert data defined by the parameters for each row and column matrix of the memory modules when applying the memory operations (column 6, lines 46-51).

As per claim 12:

Crouch et al. teaches the system of claim 9, wherein the parameters include a rippling row field to direct the sequencers to apply the memory operations to the memory modules in a column-wise fashion by holding a column address for each of the memory modules constant and rippling a row address for each of the memory modules (column 4, lines 47-51).

As per claim 13:

Crouch et al. teaches the system of claim 9, wherein the parameters include an invert rows field to direct the sequencers to invert data defined by the parameters for neighboring rows of the memory modules when applying the memory operations (column 6, lines 46-51).

As per claim 14:

Crouch et al. teaches the system of claim 9, wherein the parameters include an invert columns field to direct the sequencers to invert data defined by the parameters for neighboring columns of the memory modules when applying the memory operations (column 6, lines 46-51).

As per claim 15:

Crouch et al. teaches the system of claim 9, wherein the parameters include a plurality of optional fields to direct the sequencers to apply multiple memory operations to each of memory addresses of the memory modules (column 4, lines 30-34).

As per claim 16:

Crouch et al. teaches the system of claim 9, wherein the parameters include a default data in field that directs the sequencers to apply an input data value to the memory modules during a read operation (column 4, lines 7-10).

As per claim 17:

Crouch et al. teaches the system of claim 7, wherein the set of defined operation codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters (column 6, lines 19-25).

As per claim 18:

Crouch et al. teaches the system of claim 7, wherein the set of defined operational code includes an operational code that directs the sequencers to test a particular one of the memory modules (column 7, lines 19-24).

As per claim 19:

Crouch et al. teaches the system of claim 9, wherein the parameters include a failure analysis field to direct the sequencers to selectively toggle between failure analysis mode and a BIST mode (columns 5-6, lines 55-6).

As per claim 20:

Crouch et al. teaches the system of claim 19, wherein when operating within the failure of analysis mode a memory identification field of the parameters directs the sequencers to select data from a specific one of the memory modules for failure analysis and a bus slice field that indicates a portion of a multiplexed data bus from the selected memory module to be used for failure analysis (Figure 4, columns 8-9, lines 62-25).

As per claim 21:

Crouch et al. teaches the system of claim 7, wherein the set of defined operational codes includes an operational code that directs at least one of the distributed sequencers to apply a memory test algorithm stored within that sequencer (column 3, lines 39-45).

As per claim 22:

Crouch et al. teaches the system of claim 1, further comprising a plurality of memory interfaces coupled between the sequencers and the memory modules, wherein the memory interfaces apply the commands to the memory modules under the direction of the sequencers and in accordance with physical characteristics of the memory module (Figure 2 "Memory 215").

As per claim 23:

Crouch et al. teaches the system of claim 1, wherein BIST controller issues the commands to the sequencers in parallel for application to the memory modules (columns 7-8, lines 56-8).

As per claim 24:

Crouch et al. teaches the system of claim 1, wherein the sequencers apply the commands to the respective memory modules in accordance with timing requirements of the memory modules (column 8, lines 51-61).

As per claim 26:

Crouch teaches a device comprising a centralized BIST control means for issuing commands that conform to a generalized command protocol and define a BIST algorithm for testing a plurality of distributed memory modules having different timing requirements and physical characteristics (column 2, lines 6-9), and distributed means for interpreting the commands and applying the commands to the memory modules in accordance with timing requirements (column 2, lines 6-9) and physical characteristics of the memory modules (Figure 2, "Memory 215"), each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at

least two of the sequencers are associated with memory modules operating on different clock domains (column 4, lines 35-50).

As per claim 27:

Crouch teaches the device of claim 26, wherein the distributed means includes interface means for generating translated address and data signals based on the physical characteristics of the memory modules to apply the BIST algorithm to the memory modules (Figure 2, "Memory 215").

As per claim 28:

Crouch teaches a method comprising directing application of an algorithm from a centralized controller by issuing generalized commands that conform to a command protocol to test a plurality of memory modules (Figure 2 # 210), and interpreting the commands with a distributed set of sequencers to apply the commands as one or more sequencers of memory operations in accordance the command protocol (Figure 2 # 210 & 225, column 5, lines 51-55), each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains (column 4, lines 35-50).

As per claim 29:

Crouch teaches the method of claim 28, wherein the generalized commands specify the algorithm without regard to physical characteristics and timing requirements of memory modules (column 6, lines 7-14).

As per claim 30:

Crouch teaches the method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include a sequencer identifier that identifies one or more of the sequencers to process the command and apply the command to the respective memory modules (column 6, lines 7-20).

As per claim 31:

Crouch teaches the method of claim 30, wherein the sequencer identifier comprises one of a broadcast identifier indicating that the command is to be interpreted (column 7, lines 1-10) and applied be all of the distributed sequencers and a unicast identifier that identifies a specific one of the sequencers to interpret the command (column 7, lines 20-26).

As per claim 32:

Crouch teaches the method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include an operational code selected from a set of defined operational codes and a set of associated parameters (column 5, lines 51-60).

As per claim 33:

Crouch teaches the method of claim 32, wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from the address and data lines used during normal operation (column 6, lines 7-10).

As per claim 34:

Crouch teaches the method of claim 32, wherein the set of defined operational codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters (column 5, lines 57-60).

As per claim 35:

Crouch teaches the method of claim 32, wherein the set of defined operational codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters (column 6, lines 19-25).

As per claim 36:

Crouch teaches the method of claim 32, wherein the set of defined operational code includes an operational code that directs the sequencers to test a particular one of the memory modules (column 7, lines 19-24).

As per claim 37:

Crouch teaches the method of claim 33, wherein the set of defined operational codes includes an operational code that directs at least one of the distributed sequencers to apply a memory test algorithm stored within that sequencer (column 3, lines 39-45).

As per claim 38:

Crouch teaches the method of claim 29, wherein issuing an algorithm comprises issuing the commands to the sequencers in parallel for application to the memory modules (columns 7-8, lines 56-8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-10, 12, 25 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ledford et al. US Pat no. 6,347,056 B1.

As per claim 1:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), are associated with memory modules operating on different clock domains (abstract, lines 7-10).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 2:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein the generalized commands specify the algorithm in accordance with the command protocol (column 3, lines 31-32) and without regard to timing requirements of the memory modules.

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these

known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 3:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein the generalized commands specify the algorithm (column 3, lines 31-32) without regard to physical characteristics of the memory modules.

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 4:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49),

wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 5:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), and wherein the

sequencer identifier comprises a broadcast identifier to indicate that the generalized command is to be interpreted and applied by all of the distributed sequencers (column 3, lines 26-30).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 6:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), and wherein the sequencer identifier comprises a unicast identifier that identifies a specific one of the

sequencers (column 4, lines 23-25) to interpret and apply the generalized command to the respective memory modules of the identified sequencer.

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 7:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), and wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes (column 2, lines 33-36) and a set of associated parameters (column 5, lines 19-25).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1.# 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 8:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes (column 2, lines 33-36) and a set of associated parameters (column 5, lines 19-25), and wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the

memory modules for testing (column 5, lines 8-15) by isolating the memory modules from address and data lines used during normal operation.

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 9:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes (column 2, lines 33-36) and a set of associated parameters (column 5, lines 19-25), wherein the set of defined operational

codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing (column 5, lines 8-15) by isolating the memory modules from address and data lines used during normal operation, and the set of defined operational codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters (column 2, lines 31-36).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 10:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that

identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes (column 2, lines 33-36) and a set of associated parameters (column 5, lines 19-25), wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing (column 5, lines 8-15) by isolating the memory modules from address and data lines used during normal operation, the set of defined operational codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters (column 2, lines 31-36), and wherein the parameters include a single-row (SR) field to direct the sequencers to apply the memory operations for all columns of the memory module of the respective memory modules for the sequencers that has a largest column-bit option while maintaining a row address at zero (column 3, lines 4-11).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these

known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 12:

Ledford et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 1 # 10, column 2, lines 29-31), that stores an algorithm for testing a plurality of memory modules (Figure 1 # 32-38, column 2, lines 45-49), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (Figure 2, column 3, lines 30-33), wherein each of the generalized commands includes a sequencer identifier (column 4, lines 37-39) that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules (column 4, lines 23-27), wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes (column 2, lines 33-36) and a set of associated parameters (column 5, lines 19-25), wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing (column 5, lines 8-15) by isolating the memory modules from address and data lines used during normal operation, the set of defined operational codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters (column 2, lines 31-36), and wherein the parameters include a rippling row field to direct the sequencers to apply the memory operations to the memory modules in a column-wise

fashion by holding a column address for each of the memory modules constant and rippling a row address for each of the memory modules (column 4, lines 47-51).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 26:

Ledford et al. substantially teaches (US Pat no. 6,347,056 B1) also teaches a device comprising a centralized BIST control means for issuing commands that conform to a generalized command protocol and define a BIST algorithm for testing a plurality of distributed memory modules having different timing requirements and physical characteristics (Figure 1, #10), and distributed means for interpreting the commands and applying the commands to the memory modules in accordance with timing requirements (Fig 3, # 72) and physical characteristics of the memory modules (Figure 1, # 32, 34, 36, 38), are associated with memory modules operating on different clock domains (abstract, lines 7-10).

Ledford et al. does not explicitly teach a plurality of sequencers that interpret the commands based on the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

As per claim 28:

Ledford et al. substantially teaches a method comprising directing application of an algorithm from a centralized controller by issuing generalized commands that conform to a command protocol to test a plurality of memory modules (Figure 1 # 32, 34, 36, 38), are associated with memory modules operating on different clock domains (abstract, lines 7-10).

Ledford et al. does not explicitly teach a distributed set of sequencers to apply the commands as one or more sequencers of memory operations in accordance the command protocol.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a memory interface (Figure 1 # 32) as a plurality of sequencers, since the examiner takes official notice of the equivalence of memory interface and a sequencer for their use memory testing and the selection of any of these known equivalents to interpret commands and apply commands to memory interfaces would be within the level of ordinary skill in the art.

Claim 25 is rejected under 35 U.S.C.103 (a) as being unpatentable over Crouch et al. US Pat no. 5,995,731, and further in view of Johnston et al. US Pat no. 6,272,588 B1.

As per claim 25:

Crouch et al. substantially teaches a system comprising a centralized built-in self-test (BIST) controller (Figure 2 # 210 column 5, lines 55-60), that stores an algorithm for testing a plurality of memory modules (Figure 2 # 210), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (column 3, lines 55-59), a plurality of sequencers that interpret the commands based on the command protocol (Figure 2 # 210 & 225, column 5, lines 51-55) and apply the generalized commands to the memory modules, wherein each of the sequencers comprises a plurality of command controllers that implement the commands in accordance with a command protocol (Figure 2), each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains (column 4, lines 35-50).

Crouch et al. does not explicitly teach a command parser to parse each of the commands to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller.

However, Johnston, in an analogous art, teaches a command parser to parse each of the commands to identify an operational code and a set of parameters based on the command protocol (column 5, lines 4-9), wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST (column 5, lines 30-39). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to teach a command parser within the sequencers of Crouch at al. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that parsing the data would have allowed the skilled artisan to separate and output the data (column 5, lines 7-9).

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 5633877 A, US Pat no. 5661732 A, US Pat no. 5675545 A, and US PG-Pub 20020199139 A1 mention the same system of testing using a BIST circuit are included herein for Applicant's review.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.S

Saqib Siddiqui
Art Unit 2138
08/18/2006

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